A Model-Based Approach to Automated Diagnosis of Multiple Parametric Faults

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Abstract - **An approach is proposed to automated diagnosis of multiple parametric faults in analog electronic circuits using *PSpice*-like circuit simulators. Based on circuit responses that well characterize the faults, the set of typical faulty variants of the circuit is simulated. The multiple fault generation is reduced to a parametric analysis of the diagnosis model of the circuit. Using post-processing of the simulation results of the diagnosis model and macro-definitions in the graphical analyzer *Probe*, a fault diagnosis of the circuit is performed. An example is given illustrating the proposed approach.**

Keywords – **Fault Modeling, Model Based Diagnosis, Parametric Faults, PSpice Simulation**

I. INTRODUCTION

The circuit diagnosis and testing are important stages in the realization of the electronic circuits. In the production of the circuits, testing can be a limiting factor, contributing significantly to manufacturing cost. The multitude of response parameters make analog circuit testing difficult and expensive. This motivates research in structured fault based approaches [1-4]. Recently, a number of approaches were developed to the circuit testability investigation by selecting the optimal groups of test nodes in order to increase the percentage of the detected faults. Different approaches are proposed to analog circuit diagnosis, based on model-based approach [5-7], branch decomposition diagnosis at subcircuit and at component level [8], symbolic analysis methods [9], optimization approaches, etc. A model-based approach is developed in [7] to automated diagnosis of single parametric (soft) faults in analog circuits, based on investigation of the time-domain responses of the circuit under test. The possibilities of the standard *PSpice*-like circuit simulators are used to perform circuit diagnosis. The large possibilities of the input language, the wide range libraries of adequate component models, as well as the possibilities of post-processing in the graphical analyzer *Probe* allow the realization of effective diagnosis algorithms.

In the present paper, an approach is proposed to automated diagnosis of multiple parametric faults in analog electronic circuits using *PSpice*-like general purpose circuit simulators. Based on circuit responses that well characterize the faults, the set of typical faulty variants of the circuit is simulated. The multiple fault generation is reduced to a parametric analysis of the diagnosis model of the circuit. Using post-processing of the simulation results of the diagnosis model and macro-definitions in the graphical analyzer *Probe*, a fault diagnosis of the circuit is performed. The models, defining multiple faults of the elements, are built in the form of parameterized library components for the *Cadence PSpice* simulator. The feasibility of this approach is demonstrated by diagnosis of a benchmark circuit.

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II. PARAMETERIZED FAULT MODELS

The parametric faults are deviations of component values, resulting in a failure of some circuit specifications. The proposed faults are deviations of ±20% and ±50% from the nominal values of the passive components. These faults seem to be distributed well enough in order to cover a possible set of typical faults [10]. Each of the passive elements is characterized by the attributes M_{20}, P_{20}, M_{50} and P_{50}, defining a deviation from the nominal value of -20%, +20%, -50% and +50% correspondingly. A fault number F_i, i = 1, 2,…, n is assigned to each of the attributes M_{20}, P_{20}, M_{50}, P_{50}, where n is the total number of the modeled single faults. F_0 corresponds to a non-faulty circuit. A parametric analysis is used for the multiple fault generation, where the parameter m is the number of the faulty groups. In case of m-fold faults, a variation is defined for m independents parameters par_i , i=1, .2 …,m.

As the *PSpice* simulator does not allow independent variation of several parameters, a new parameter *par* is used for the fault generation. The variation of *par* is defined in the range 1, 2, …, n^m. The modulo function $mod(a,b)$ finding the remainder of division of a by b is used to obtain the group (par_{i1}, par_{i2}, par_{im}) corresponding to m-fold fault in the elements q_{i1}, q_{i2}, …q_{im} :

$$\mathrm{mod}(a,b)=\frac{b}{\pi}\left(\arctan\left(\tan\left(\left(\frac{a}{b}\right)\pi-\frac{\pi}{2}\right)+\frac{\pi}{2}\right)\right) \quad (1)$$

For example, if m=3, the parameters (par_{i1}, par_{i2}, par_{i3}) are obtained in the form:

$$par_1=\mathrm{mod}\left(par,n\right)\ ;\quad par_{1a}=n^2\,\mathrm{mod}\left(par,n^2\right) \quad (1)$$

$$par_2=\frac{par_{1a}-par_1}{n}\ ;\qquad par_3=\frac{par-par_{1a}}{n^2} \quad (2)$$

III. AUTOMATED FAULT DIAGNOSIS APPROACH USING PSPICE

The realization in *PSpice* is performed using the pseudocomponent PARAMETERS in the form:

```
.PARAM  pi=3.14159265
+  par1={n*(atan(tan((par/n)*pi-pi/2))+pi/2)/pi}
+  par1a = {n*n*(atan(tan((par/(n*n))*pi-pi/2))+pi/2)/pi}
+  par2= {(par1a-par1)/n}  , par3={(par-par1a)/(n*n)}
```

The parameters par_1, par_2 and par_3 can be represented in the model as node voltages and can be visualized in *Probe* using the macros:

```
p1= max(V(par1))
p2= max(V(par2))
p3= max(V(par3))
```

The results for the generated faulty elements groups for n=10 and m=3 are shown in Fig. 1.

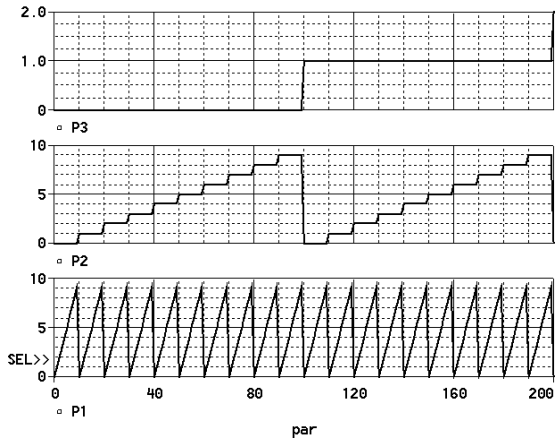


Fig. 1. Generation of the faulty element groups

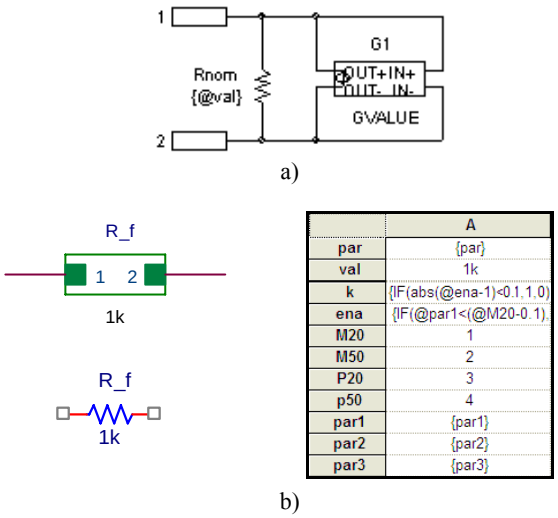


Fig. 2. Parameterized model of the faulty resistor a) subcircuit definition b) block definition

A. Model of Faulty Resistor

The model of a faulty resistor $R_f = R_{nom} + \Delta R$ is shown in Fig.1a, where the voltage controlled current source (VCCS) G1 models the deviation from the nominal value R_{nom} in the case of a fault. The value of the controlling parameter of VCCS Δg is represented in Table 1 with respect to the deviation from the nominal value. The computer realization of the faulty resistor model is performed in the graphical editor *Cadence Capture* using a block definition as shown in Fig. 1b. The fault ΔR is simulated using the VCCS of GVALUE type in Fig. 1a. If the parameter par_i is equal to the ID number of the fault in the element R, a current $\Delta I_R = \Delta g.V_{12}$ of the VCCS is defined, corresponding the this fault. It is calculated in *PSpice* according to Table 1 using the function CPGR in the form:

```
.func CPGR(x,M20,M50,P20,P50,v) {if(abs(M20-x)<0.1,
0.25/v,if(abs(M50-x)<0.1,1/v,if(abs(P20-x)<0.1,-1/(6*v),
if(abs(P50-x)<0.1,-1/(3*v),0))))}
```

where x is the fault number and v is the nominal value of R.

TABLE 1. VALUES FOR THE CONTROLLING PARAMETER IN THE RESISTOR MODEL

R_f	Δg
R_{nom}–20%R_{nom}	0.25/ R_{nom}
R_{nom}–50%R_{nom}	1/ R_{nom}
R_{nom}+20%R_{nom}	–1/(6 R_{nom})
R_{nom}+50%R_{nom}	–1/(3 R_{nom})
R_{nom}	0

In order to select the faulty group $(q_{i1}, q_{i2}, \ldots q_{im})$, the parameters ena_i , ena_i and k are calculated:

- parameter ena_i =1 if the fault number par_i is equal to the ID number of the fault.
- parameter *ena*

$$ena = \sum_{i=1}^{m} ena_i \qquad (4)$$

- parameter k =1 if ena = 1 otherwise k = 0.

As a result, k = 1 if the element is included in the tested group, otherwise k = 0.

The coefficient k multiplies the current ΔI_R in (4). Hence the fault is modeled only for the elements in the tested group.

As a result, in case of multiple fault, the current ΔI_R is

$$\Delta I_R = \sum_{i=1}^{m} k.\Delta g_i V_{12} \qquad (5)$$

For the case of three-fold fault, *ena* has the form:

```
ena = {IF(@par1<(@M20-0.1),0,IF(@par1>(@P50+0.1),
0,1))+IF(@par2<(@M20-0.1),0,IF(@par2> (@P50+0.1),
0,1))+IF(@par3<(@M20-0.1),0,IF(@par3>(@P50+0.1),0,1))}
```

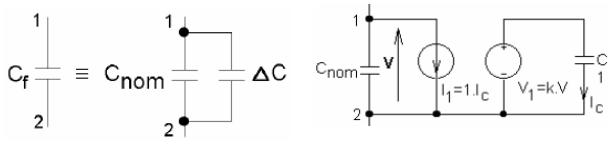
The coefficient k has the form:

k = {IF(abs(@ena-1)<0.1,1,0)}

B. Model of Faulty Capacitor

The model of a faulty capacitor $C_f = C_{nom} + \Delta C$ is shown in Fig. 3a, where the element ΔC models the deviation from the nominal value in case of a fault. The model of ΔC is shown in Fig. 3b [7]. The current controlled current source (CCCS) I1=1.I_C and the voltage controlled voltage source (VCVS) $V_1 = \Delta k . V_{12}$ model the component equation of the element ΔC .

The computer realization of the faulty capacitor model is performed in the graphical editor *Cadence Capture* using a block definition as shown in Fig. 4. The voltage controlled voltage source of EVALUE type is used to define the controlling parameter Δk modeling the fault. The value of the parameter Δk depends on the deviation. It is shown in Table 2. This source type allows the inclusion of the IF_THEN_ELSE statement in the expression in order to define the corresponding deviation.

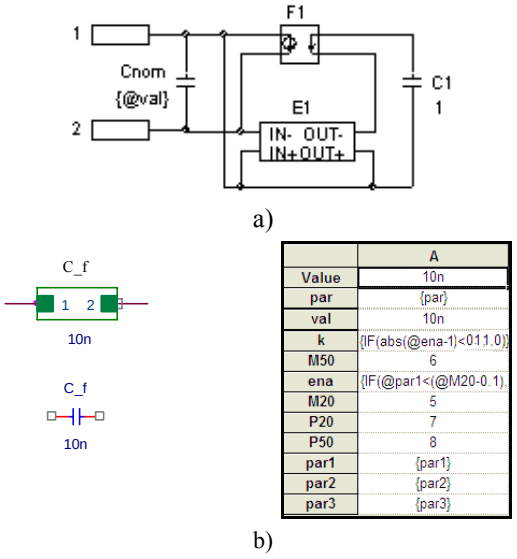


a) b)

Fig. 3. Model of Faulty Capacitor

TABLE 2. VALUES FOR THE CONTROLLING PARAMETER IN THE CAPACITOR MODEL

C_f	Δk
C_{nom}–20%C_{nom}	–0.2C_{nom}
C_{nom}–50%C_{nom}	–0.5C_{nom}
C_{nom}+20%C_{nom}	0.2C_{nom}
C_{nom}+50%C_{nom}	0.5C_{nom}
C_{nom}	0



a)

b)

Fig. 4 Parameterized model of the faulty capacitor
a) subcircuit definition b) block definition

If the parameter par_i is equal to the ID number of the fault in the element C, a voltage $\Delta E_C = \Delta k.V_{12}$ of the VCCS is defined, corresponding the this fault. It is calculated in *PSpice* according to Table 2 defining the function CPEC in the form:

.func CPEC(x,M20,M50,P20,P50,v) {if(abs(M20-x)<0.1,-0.2*v,if(abs(M50-x)<0.1,-0.5*v,if(abs(P20-x) <0.1, 0.2*v,if(abs(P50-x)<0.1,0.5*v,0)))))}

where x is the fault number.

In case of multiple fault, the voltage ΔE_C is:

$$\Delta E_C = \sum_{i=1}^{m} k.\Delta k_i V_{12} \quad , \tag{6}$$

where $k = 1$ if the element is included in the tested group, otherwise $k = 0$.

IV. DIAGNOSIS OF EXAMPLE CIRCUIT

Diagnosis of benchmark circuit of the biquadratic filter shown in Fig. 5 [7,10] is performed. The tested responses in the frequency domain are the bandwidth B, the output voltage at lower frequencies V_{low} and the maximal output voltage: V_{max}. A double fault of the elements R_3 and C_2 is assumed: R_3-20% and C_3+50%.

The measured responses of the circuit under test are: B_m = 11.076kHz, V_{lowm} = 0.8 V and V_{maxm} = 0.8949V. They are introduced in the diagnosis model using independent voltage sources of *VAC* type in the field ACMAG (Fig. 6).

The parameters B_m , V_{lowm} , V_{maxm} and the ripple R_{ipm}=V_{maxm}–V_{lowm} are obtained in *Probe* using the following macros:

```
Bm = max(Vm(B_m))
Vlowm = max(Vm(Vlow_m))
Vmaxm = max(Vm(Vmax_m))
Ripm = Vmaxm-Vlowm
```

The responses B_d, V_{mind} , V_{maxd} and R_{ipd} of the diagnosis model N_d of the faulty circuit are obtained in *Probe* using the macros:

```
Bd = LPBW(Vdb(outd),3)
F1 = MIN(Frequency)
Vlowd = YatX(Vm(outd),F1)
Vmaxd=max(Vm(outd))
Ripd = Vmaxd-Vlowd
```

The measure "distance" is calculated characterizing the relative deviation of the measured value of the response of the tested circuit with respect to the simulated value of the diagnosis model [7,10].

$$DIST_B = abs\left(1 - \frac{B_m}{B_d}\right);\ DIST_{Vlow} = abs\left(1 - \frac{V_{lowm}}{V_{lowd}}\right), \tag{7}$$

$$DIST_{Rip} = abs\left(1 - \frac{Rip_m}{Rip_d}\right) \tag{8}$$

Finally, the measure *DIST* is calculated as a root mean square value of $DIST_B$, $DIST_{Vlow}$ and $DIST_{Rip}$:

$$DIST = \sqrt{DIST_B^2 + DIST_{Vlow}^2 + DIST_{Rip}^2} \tag{9}$$

The macros for determination of *DIST* have the form:

```
DistB = abs(1-Bm/Bd)
DistVlow = abs(1-Vlowm/Vlowd)
DistVmax = abs(1-Vmaxm/Vmaxd)
DistRip = abs(1-Ripm/Ripd)
DIST = SQRT(DISTB*DISTB+
   DISTVlow*DISTVlow+DISTRip*DISTRip)
```

The ID numbers of faults p_1, p_2 and p_3 and the dependence *DIST*(*par*) are visualised in *Probe* as shown in Fig. 7 and the minimal value $DIST_{min}$ is obtained. The argument *par*, corresponding to the minimal distance between the measured and simulated values of the diagnosis model, defines the faulty variant.

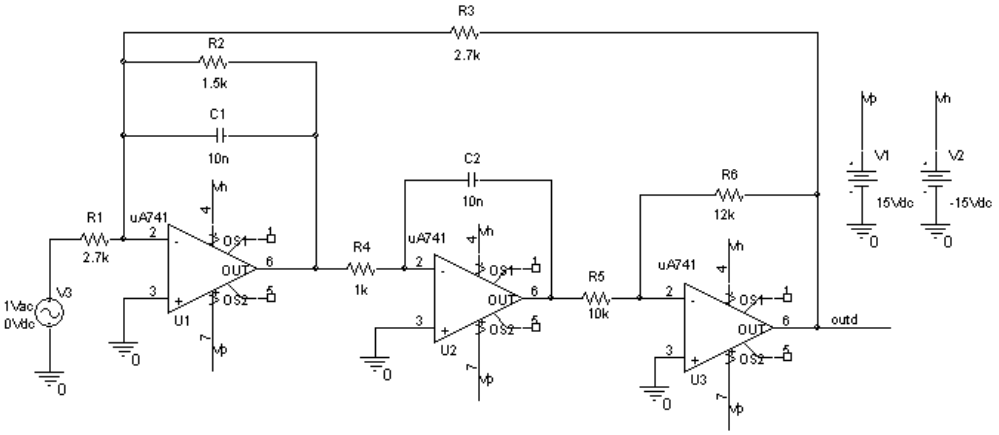


Fig. 5. Example benchmark circuit

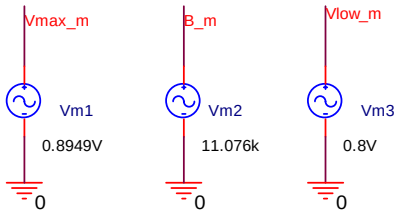


Fig. 6. Introducing the responses of the tested circuit in the model

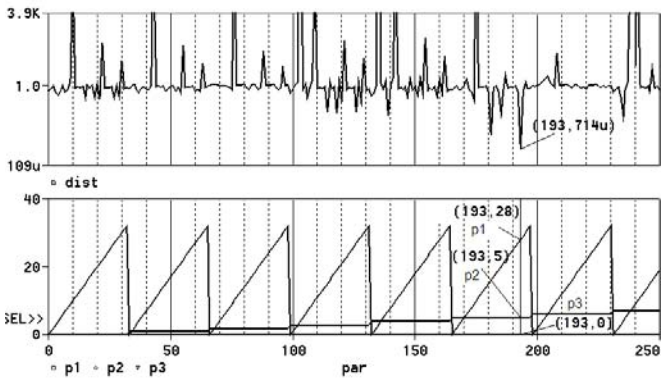


Fig. 7. The dependence of the measure *DIST* on *par*

For the case shown in Fig. 7, $DIST_{min} = 0.714 \times 10^{-3}$ for $par = 193$. Hence p_1=28, p_2=5 and p_3=0 corresponding to a double fault (R_3, C_2) : R_3–20% and C_2+50%.

V. Conclusion

An approach has been developed to automated diagnosis of multiple parametric faults in analog electronic circuits using *PSpice*-like circuit simulators. Parametric analysis of a diagnosis model of the faulty circuit is used for the multiple fault generation. The measures that characterize the distance between the measured test characteristics of the faulty circuit and the diagnosis model are obtained in *Probe*. Using post-processing of the simulation results by macro-definitions in *Probe*, a fault diagnosis of the circuit is performed. Parameterized macromodels of the faulty components are built. The feasibility of the proposed approach is demonstrated by diagnosis of a benchmark circuit.

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